

FIG.1

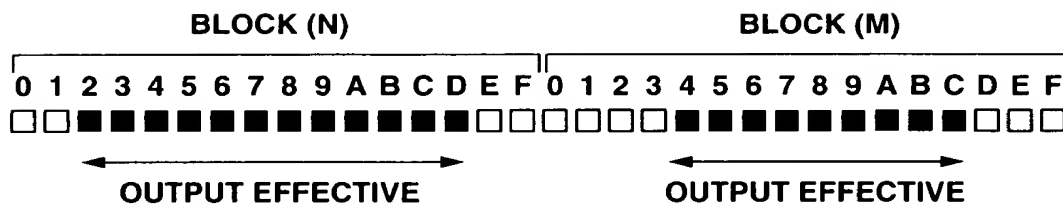


FIG.2

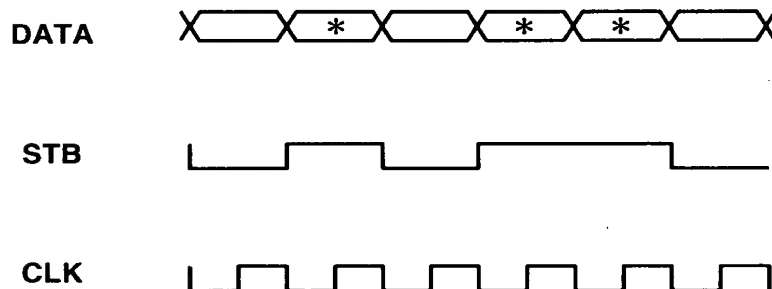
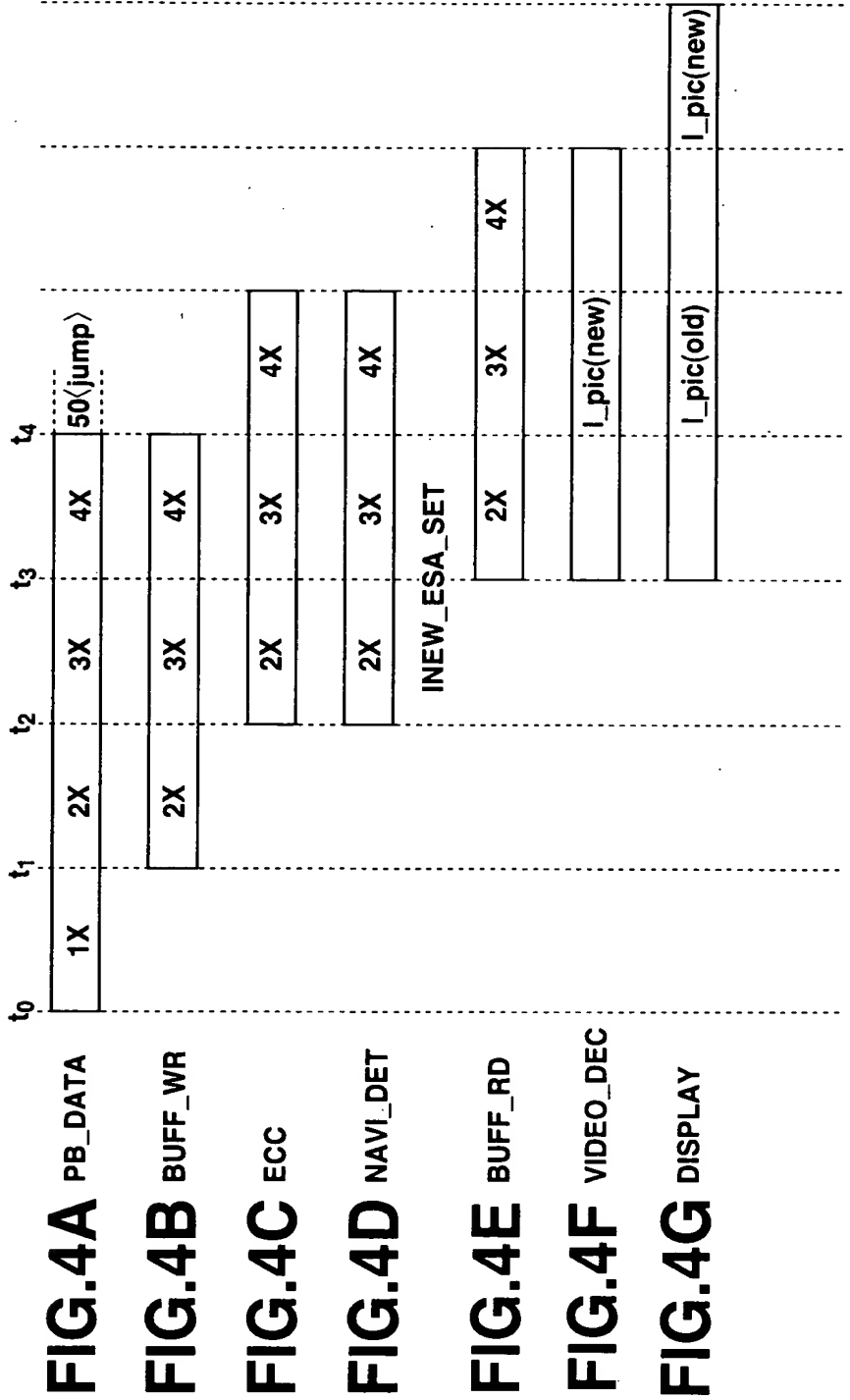
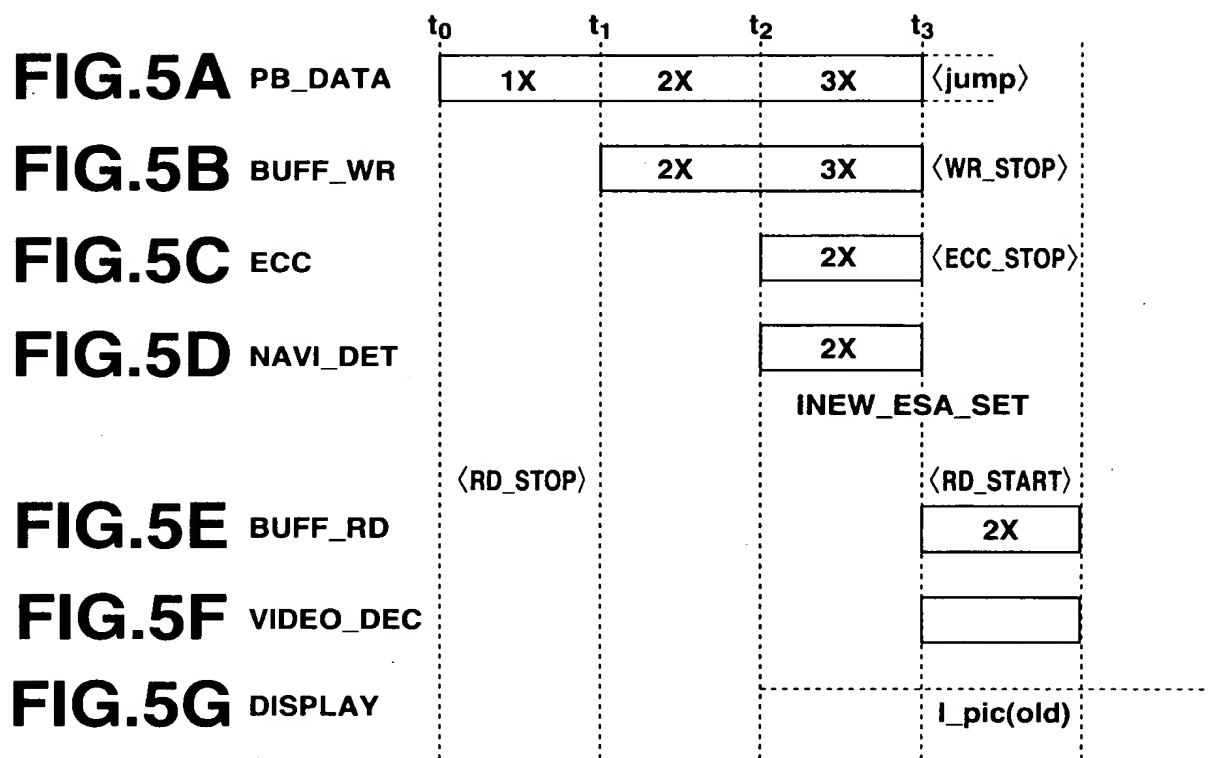


FIG.3





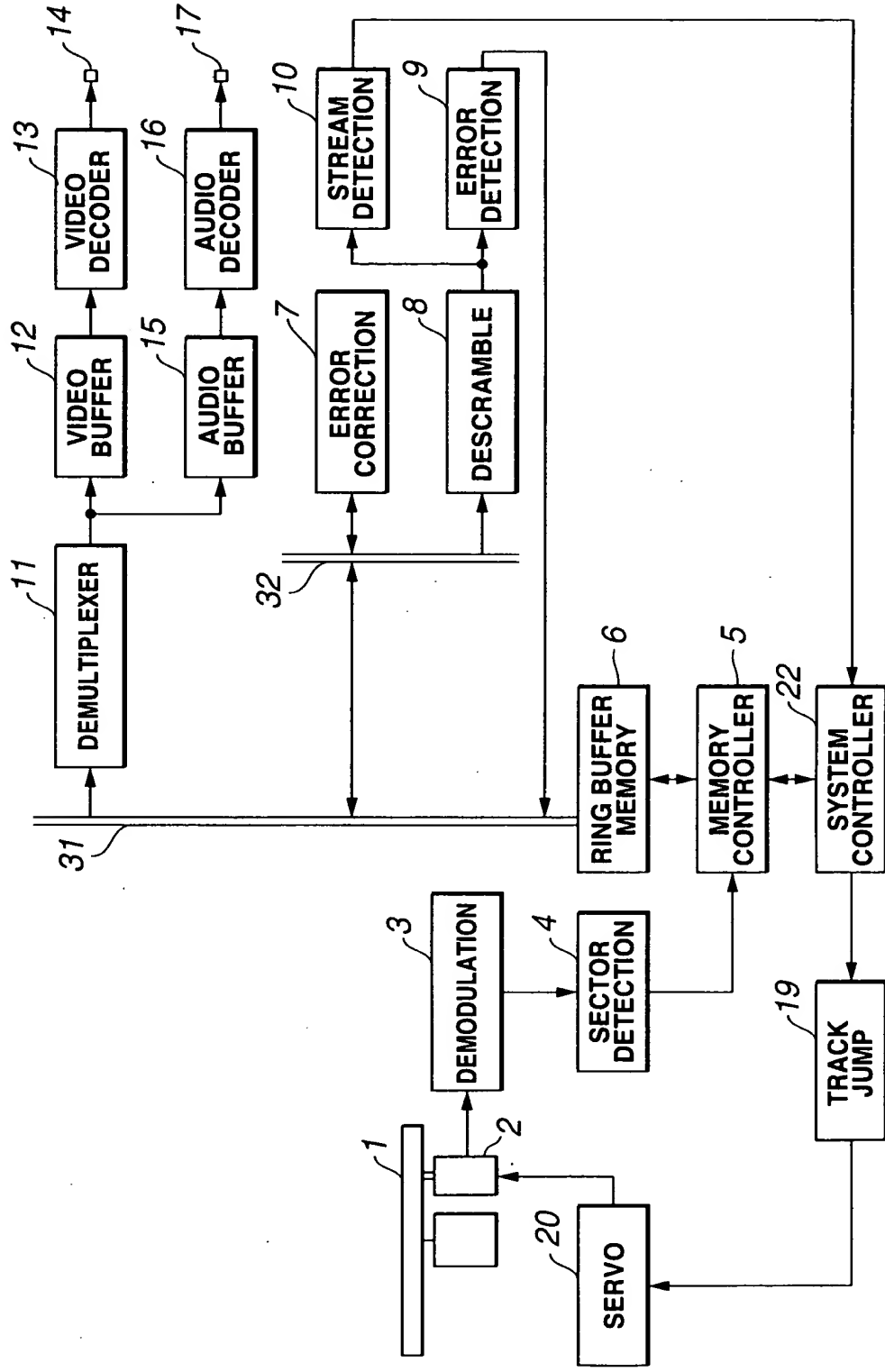


FIG.6

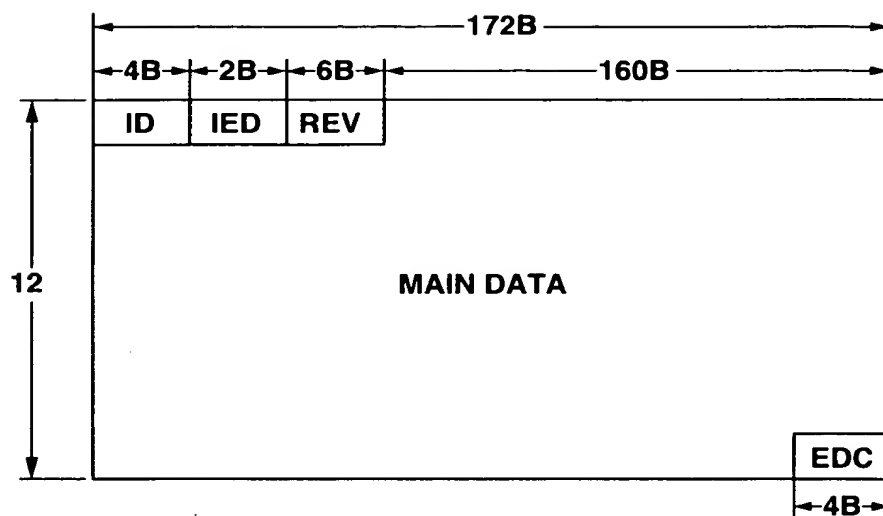


FIG.7

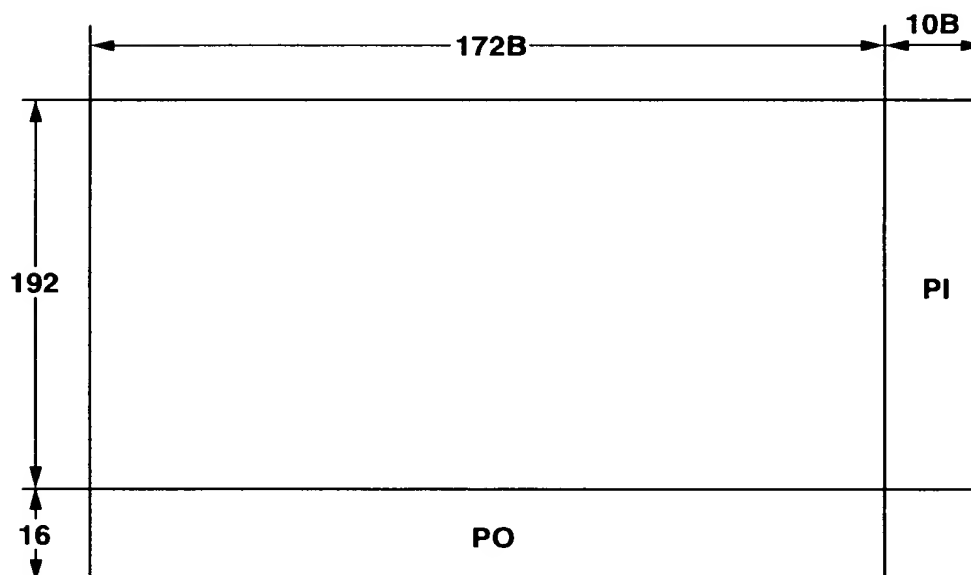


FIG.8

00520F" 00050960

32BITS		1456BITS		32BITS		1458BITS	
SY0	ID IED			SY5			P1
SY1				SY5			P1
SY2				SY5			P1
SY3				SY5			P1
SY4				SY5			P1
SY1				SY6			P1
SY2				SY6			P1
SY3				SY6			P1
SY4				SY6			P1
SY1				SY7			P1
SY2				SY7			P1
SY3				SY7			EDC P1
SY4		P0		SY7			P0 P1

FIG.9

0050500 10500

FIG.10A

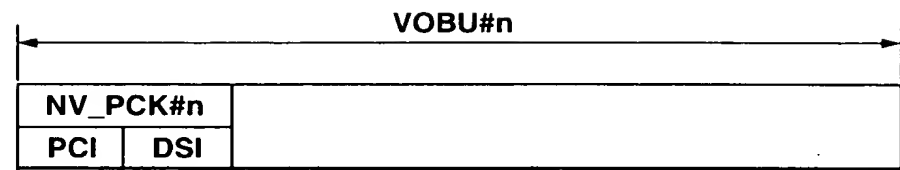


FIG.10B

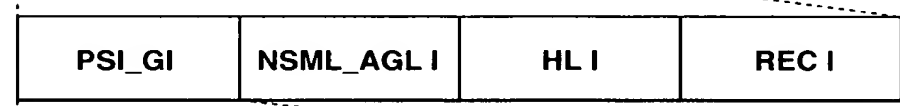


FIG.10C

	Content
(1)NV_PCK_LBN	LBN of Navigation pack
(2)VOBU_CAT	Category of VOBUn
reserved	reserved
(3)VOBU_UOP_CTL	User Operation control of VOBUn
(4)VOBU_S_PTM	Start PTM of VOBUn
(5)VOBU_E_PTM	End PTM of VOBUn
(6)VOBU_SE_E_PTM	Eun PTM of scqurnce end in VOBUn
(7)C_SLIM	Cell Elpse Time

FIG.11A

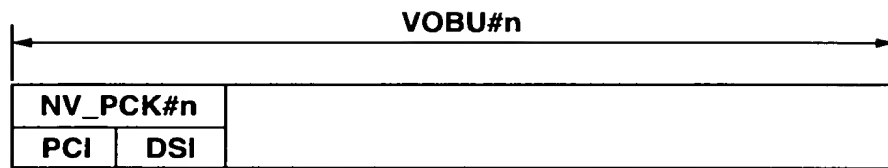


FIG.11B



FIG.11C

	Content
(1)NV_PCK_SCR	SCR_base of NV_PCK
(2)NV_PCK_LBN	LBN of NV_PCK
(3)VOBU_EA	End address of VOB
(4)VOBU_1STREF_EA	End address of the first Reference Picture in VOB
(5)VOBU_2NDREF_EA	End address of the second Reference Picture in VOB
(6)VOBU_3RDREF_EA	End address of the third Reference Picture in VOB
(7)VOBU_VOB_I DN	VOB ID number of the VOB
reserved	reserved
(8)VOBU_C_I DN	Cell ID number of the VOB
(9)C_ELTIM	Cell Elpse Time

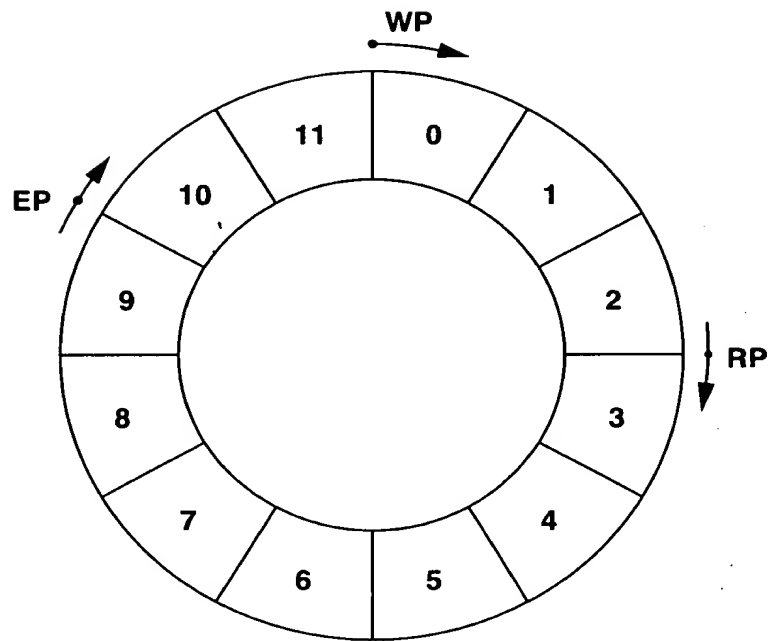


FIG.12

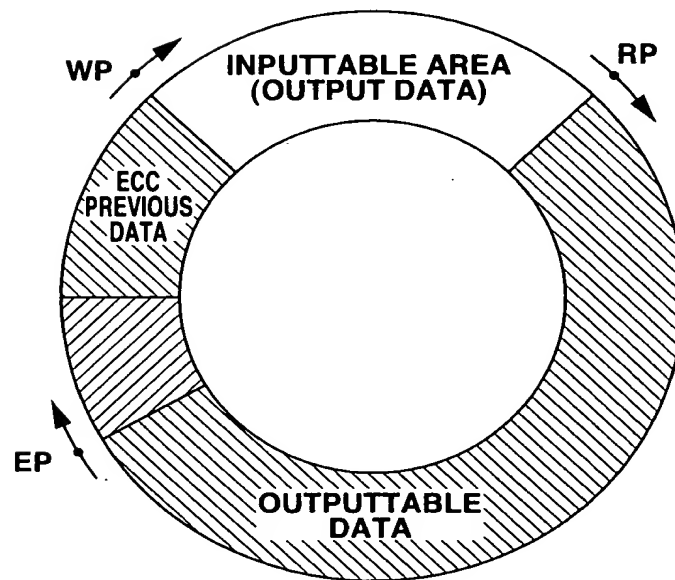


FIG.13

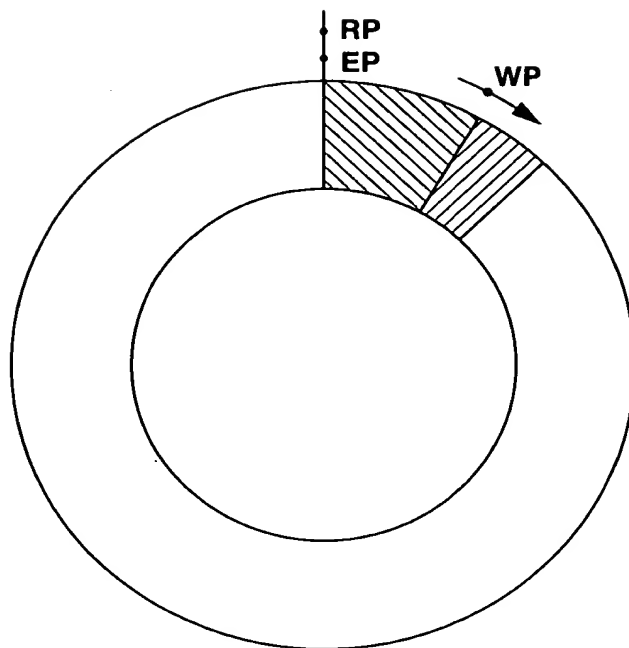


FIG.14

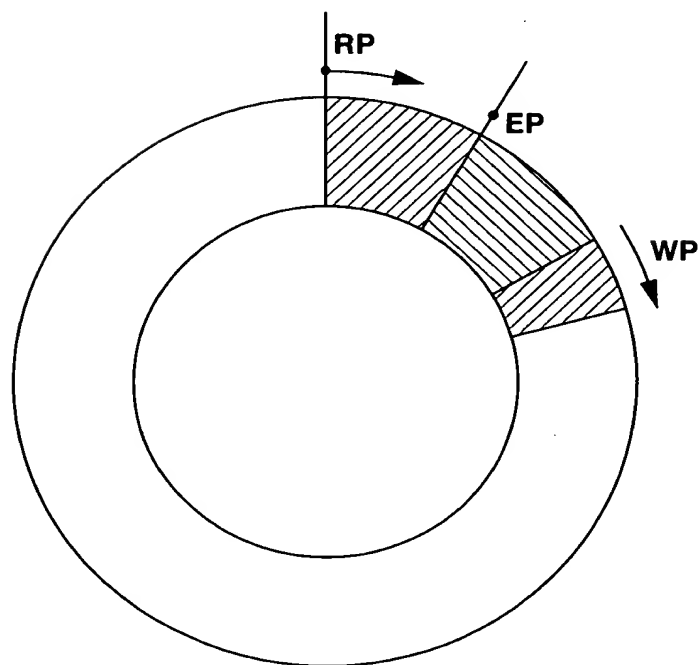


FIG.15

0050509 102500

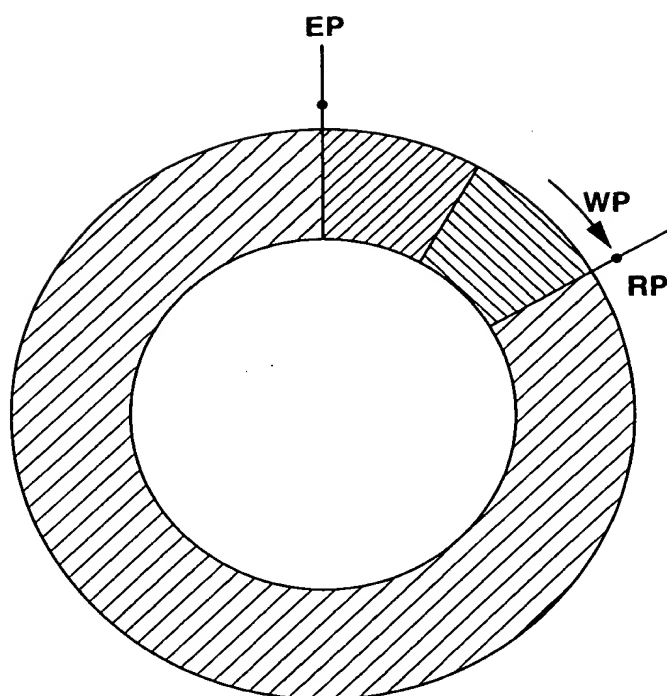


FIG.16

FIG.17A

BUFF_WR

BLOCK (N) BLOCK (N+1)



FIG.17B

START SECTOR

FIG.17C

END SECTOR

FIG.17D

OUTPUT SPECIFYING SECTOR

FIG.17E

NAVI SECTOR

FIG.17F

CORRECTION RESULT FLAG

FIG.17G

IP OUTPUT SECTOR

FIG.17H

BUFF_RD



FIG.18A BUFF_WR

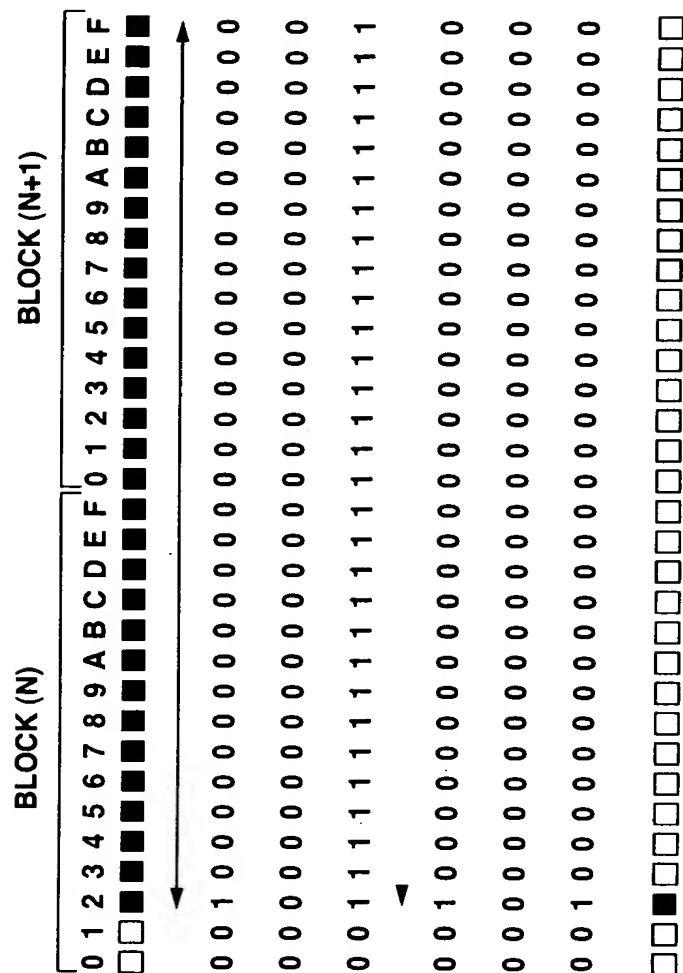


FIG.18B START SECTOR

FIG.18C END SECTOR

FIG.18D OUTPUT SPECIFYING SECTOR

FIG.18E NAVI SECTOR

FIG.18F CORRECTION RESULT FLAG

FIG.18G IP OUTPUT SECTOR

FIG.18H BUFF_RD

Timing diagram for the IPI interrupt sequence. The diagram shows a sequence of events over time, marked by vertical dashed lines at t_0 , t_1 , t_2 , t_3 , and t_4 .

- At t_0 , a '1X' pulse occurs.
- At t_1 , a '2X' pulse occurs.
- At t_2 , a '3X' pulse occurs.
- At t_3 , a 'jump' signal is asserted, followed by 'WR_STOP' and 'ECC_STOP' signals.
- At t_4 , the 'IPI_END_DET' signal is asserted.

The 'IPI_END_DET' signal is shown as a pulse that starts at t_3 and ends at t_4 .